

# Compal Confidential

## Cougar

### Schematics Document

#### Intel Cedar Trail Processor/ Tiger point

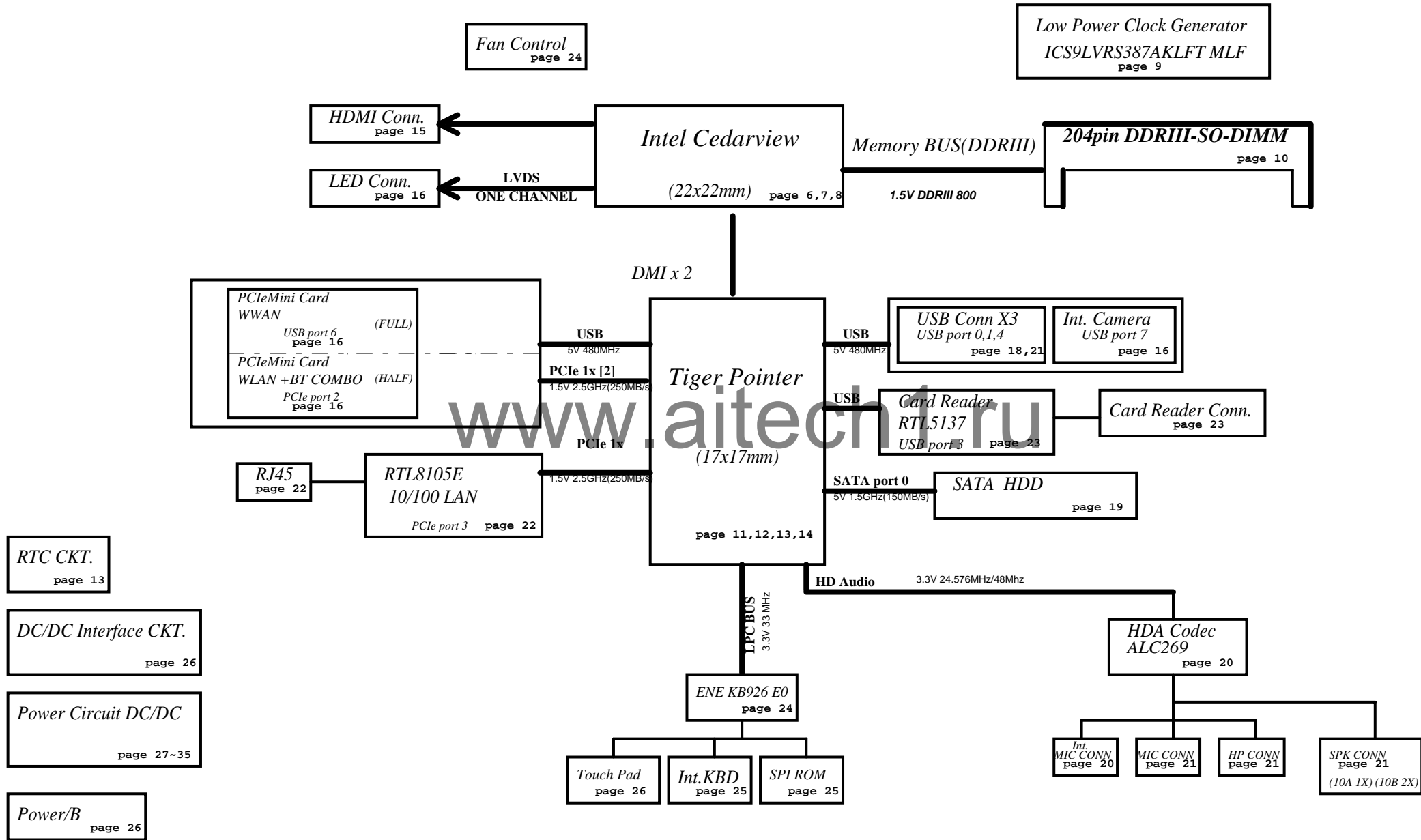
2010-11-05

REV:0.1

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Model Name : PBU00  
File Name : P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

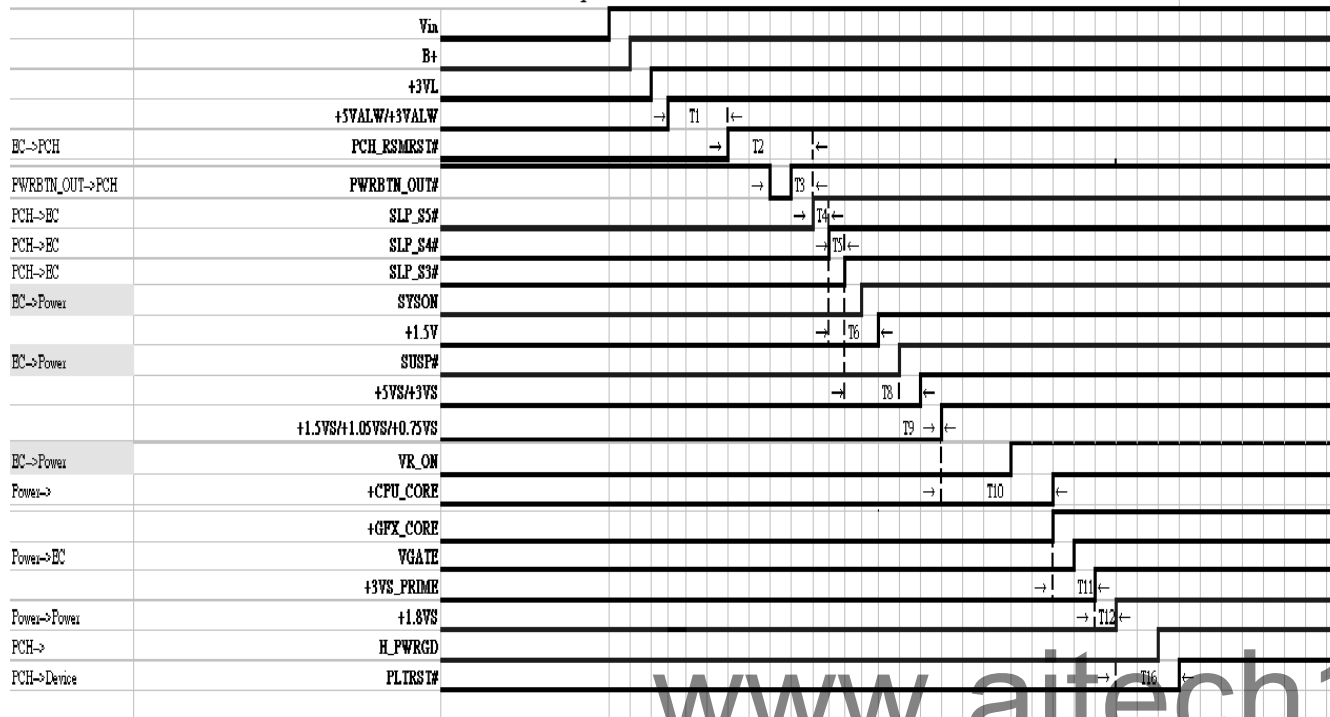
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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## PBU00 Power ON sequence

2010/7/2



## Power-on Sequence

Time	Description	Expected
T1	+5VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	"
T4	SLP_S5# inactive to SLP_S4# inactive	28.992ms ~ 64.088ms
T5	SLP_S4# inactive to SLP_S3# inactive	28.992ms ~ 64.088ms
T6	SLP_S3# inactive to +1.5V active	"
T8	SLP_S5# inactive to +5VS inactive	"
T9	+1.5V active to +1.05V active	"
T10	+1.05V active to +CPU_CORE	"
T11	+CPU_CORE active to +3.3V_PRIME	"
T12	+3.3V_PRIME active to +1.8V	3.3-1.8<700mV
T16	H_PWRGD inactive to PLTRST# inactive	34<RTCCCLK[4]

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# Cougar Power Map

B+

DESIGN CURRENT 250mA

Ipeak=6.97A, Imax=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

UP6182CQAG

\*\* The SW just is reserved.  
The power passes by jump or  
0-ohm resistor.

WOL\_EN#

\*\* P-CHANNEL  
AO3413

DESIGN CURRENT 300mA

+3V\_LAN

Ipeak=3.98A, Imax=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 2286mA

+5VS

VGATE

APL5930KA

DESIGN CURRENT 151mA

+1.8VS

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL  
AO3413

DESIGN CURRENT 2000mA

+LCD\_VDD

VGATE#

N-CHANNEL  
SI4800BDY

DESIGN CURRENT 294mA

+3VS\_PRIME

SUSP#

SY8033BDBC

Ipeak=1.308A, Imax=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR\_ON

RT8165BGQW

Imax=3.5A

DESIGN CURRENT 4500mA

+CPU\_COREP

DESIGN CURRENT 2000mA

+GFX\_COREP

SYSON

G5603RU1U

Ipeak=19.6A, Imax=13.72A

DESIGN CURRENT 2270mA

+1.5VP +-5%

SUSP#

IRF8113PBF

DESIGN CURRENT 2112mA

+1.5VSP

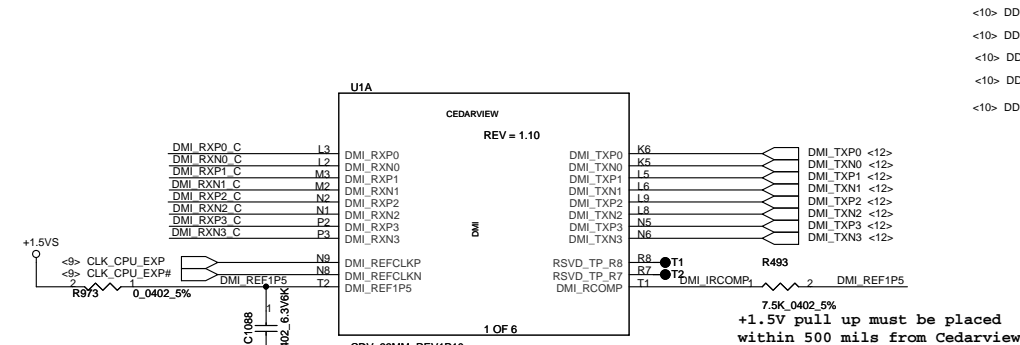
SUSP

UP7711U8

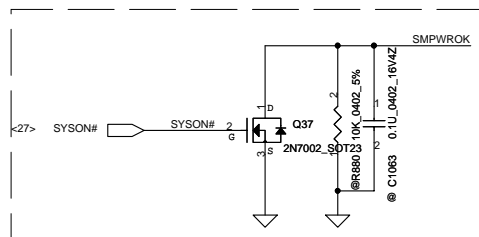
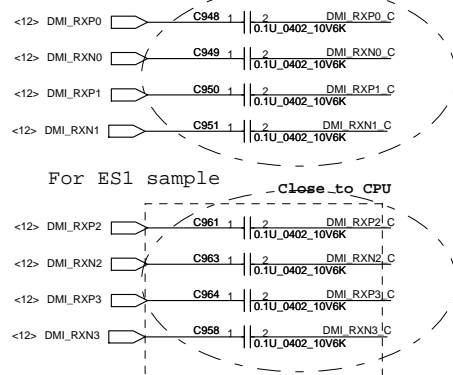
DESIGN CURRENT 500mA

+0.75VSP

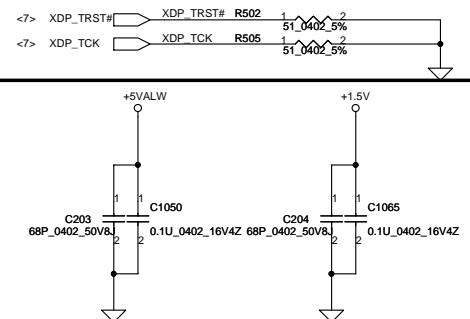
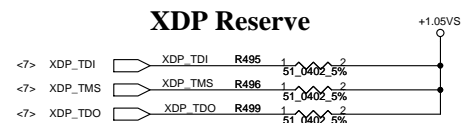
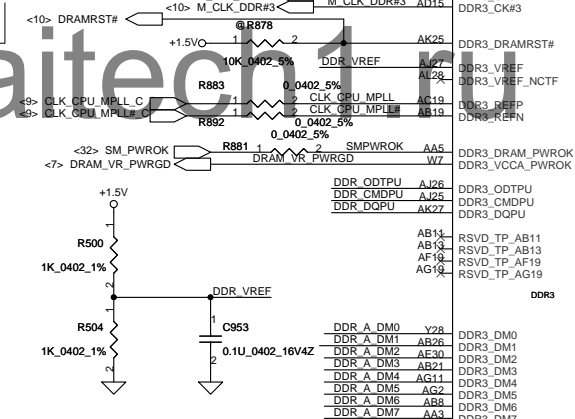
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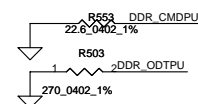
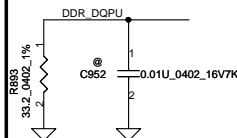
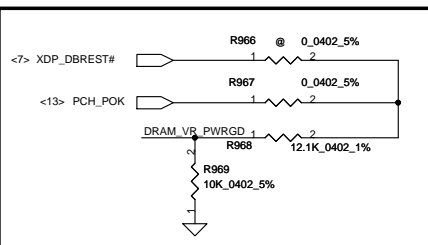
**+1.5V pull up must be placed within 500 mils from Cedarview**



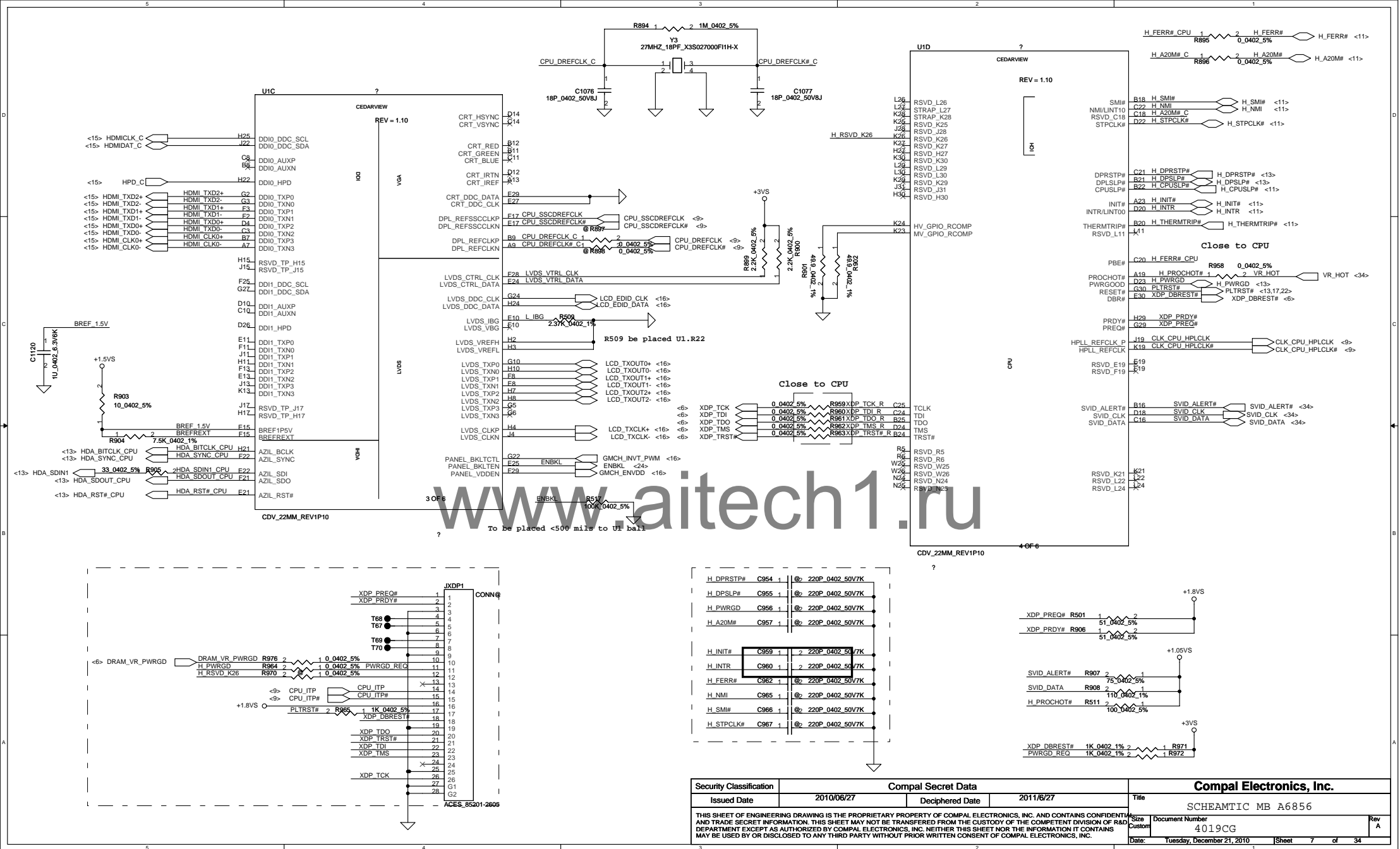
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**Reserve PM\_SLP\_S4# to turn on DRAM\_PWROK**



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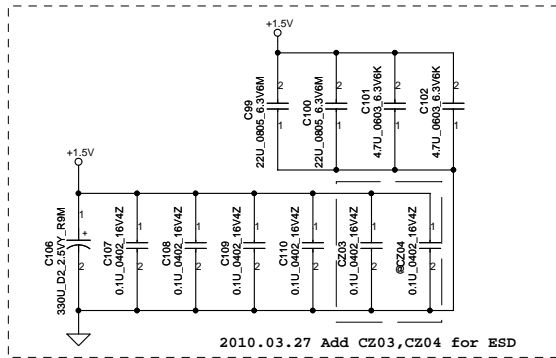






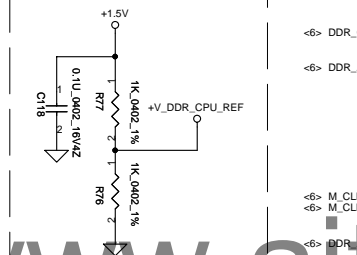
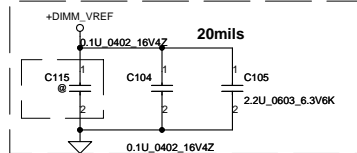
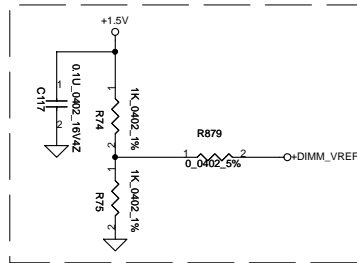
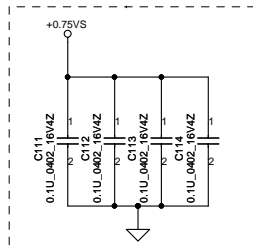
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 <6> DDR\_A\_D[0..63]  
 <6> DDR\_A\_DM[0..7]  
 <6> DDR\_A\_DQS[0..7]  
 <6> DDR\_A\_MA[0..14]

Layout Note:  
 Place near JDDR1



2010.03.27 Add C203,C204 for ESD

Layout Note:  
 Place one cap close to every 2 pullup resistors terminated to +0.75VS



<6> DDR\_CKE2

<6> DDR\_A\_BS2

<6> M\_CLK\_DDR2

<6> M\_CLK\_DDR#2

<6> DDR\_A\_BS0

<6> DDR\_A\_WE#

<6> DDR\_A\_CAS#

<6> DDR\_A\_MA13

<6> DDR\_CS3#

<6> M\_CLK\_DDR3

<6> M\_CLK\_DDR#3

<6> DDR\_A\_BS1

<6> DDR\_A\_RAS#

<6> DDR\_CS2#

<6> M\_ODT2

<6> M\_ODT3

<6> M\_ODT3 <6> +VREF\_CA

<6> DDR\_A\_D37

<6> DDR\_A\_D32

<6> DDR\_A\_DQS#4

<6> DDR\_A\_DQS4

<6> DDR\_A\_D34

<6> DDR\_A\_D35

<6> DDR\_A\_D41

<6> DDR\_A\_D44

<6> DDR\_A\_D45

<6> DDR\_A\_D49

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<6> DDR\_DM7

<6> DDR\_A\_D58

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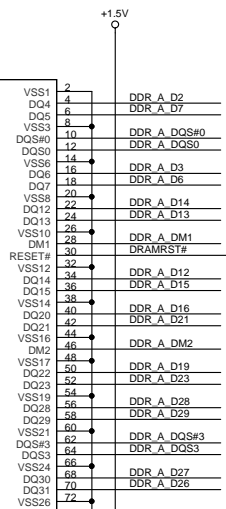
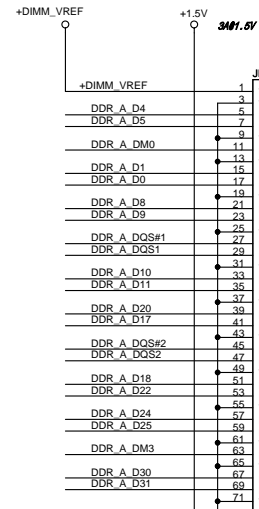
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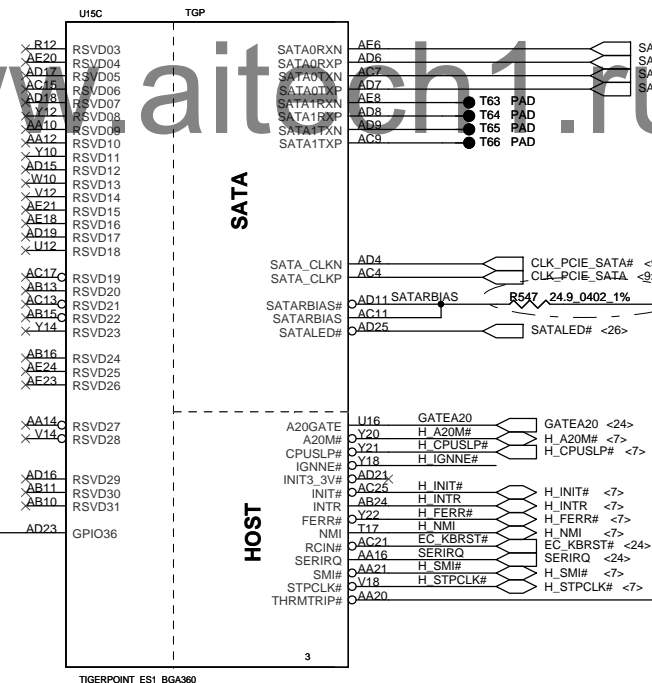
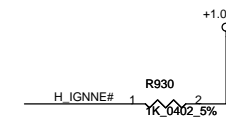
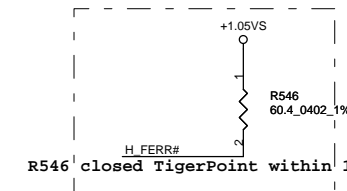
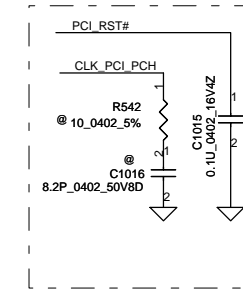
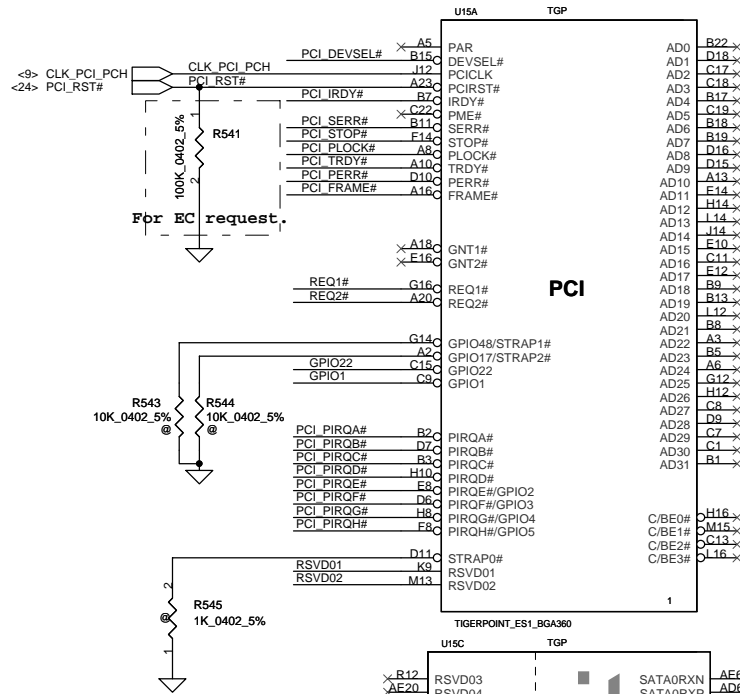
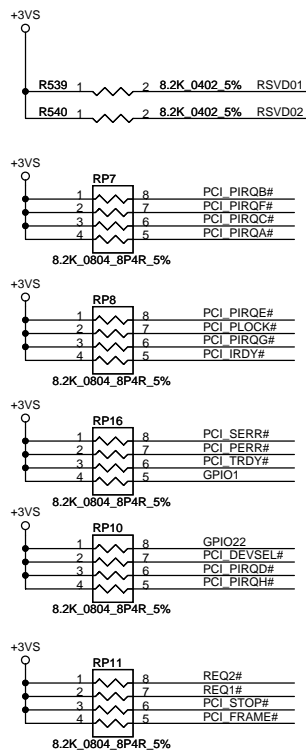
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<6> DDR\_A\_D80

<6> DDR\_A\_D81

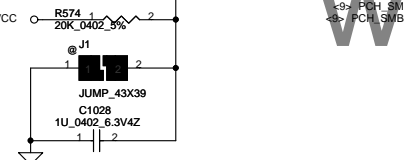
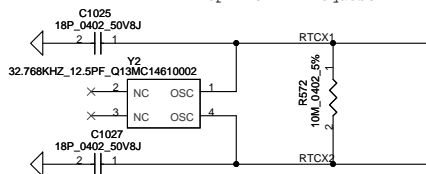
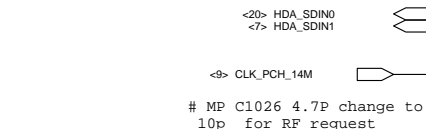
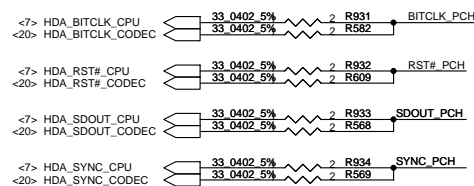
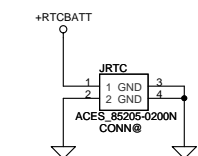
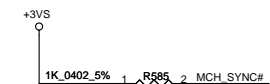
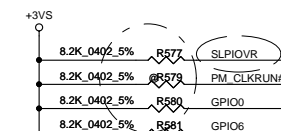
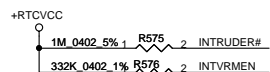
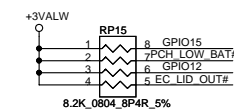
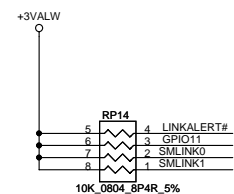
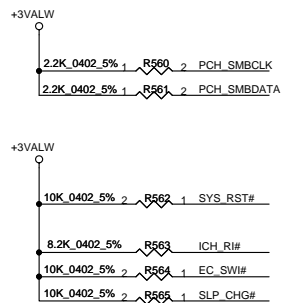
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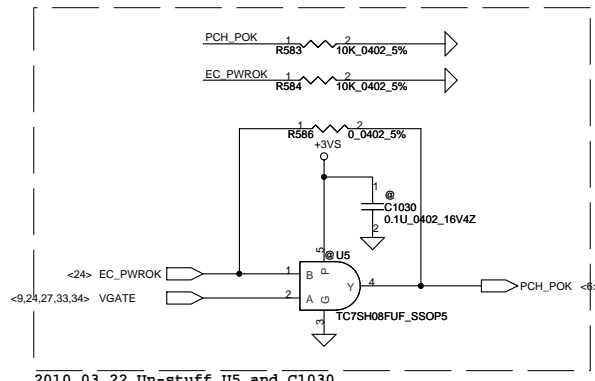
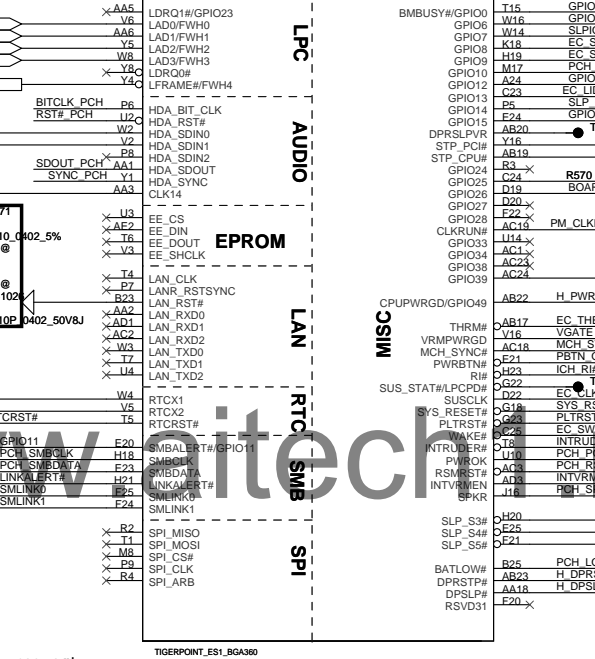
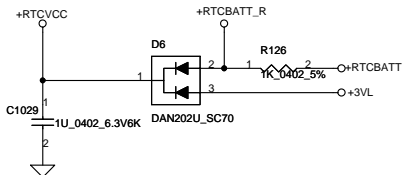


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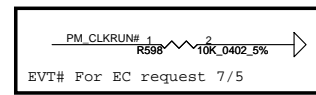




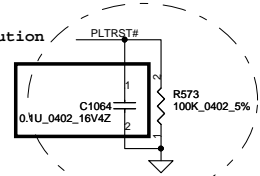
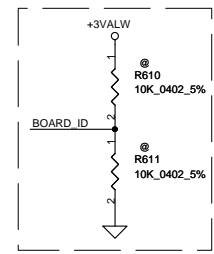
7/20 Add SLPIOV# pull up 8.2k to +3vs  
9/23 Change RP17 to R256, R257, R258 for layout request



2010.03.22 Un-stuff U5 and C1030



EVT# For EC request 7/5



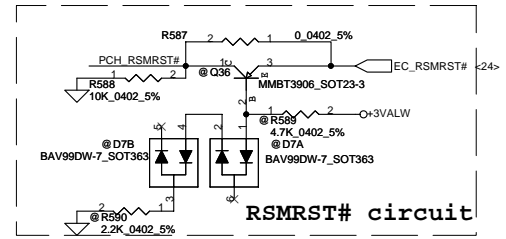
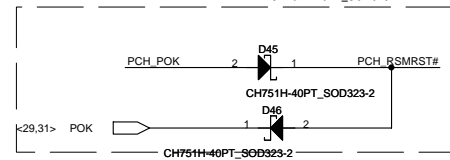
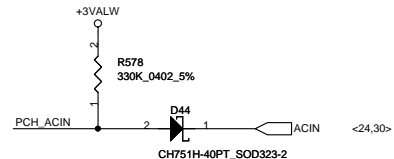
12/31 Add HW Board ID function

2010.04.22 Add C1064 for ESD solution

7/20 Add test point

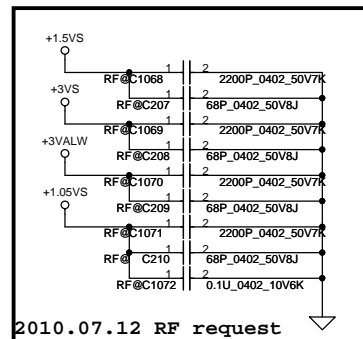
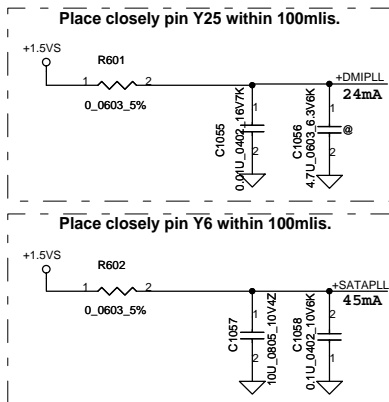
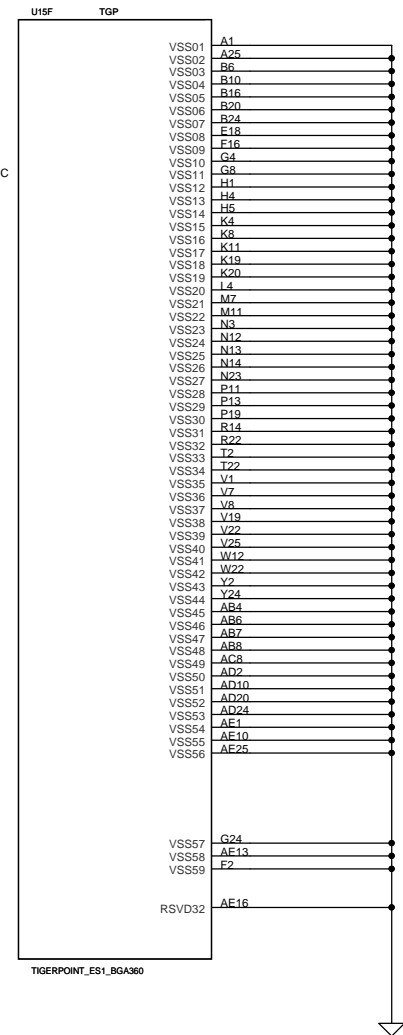
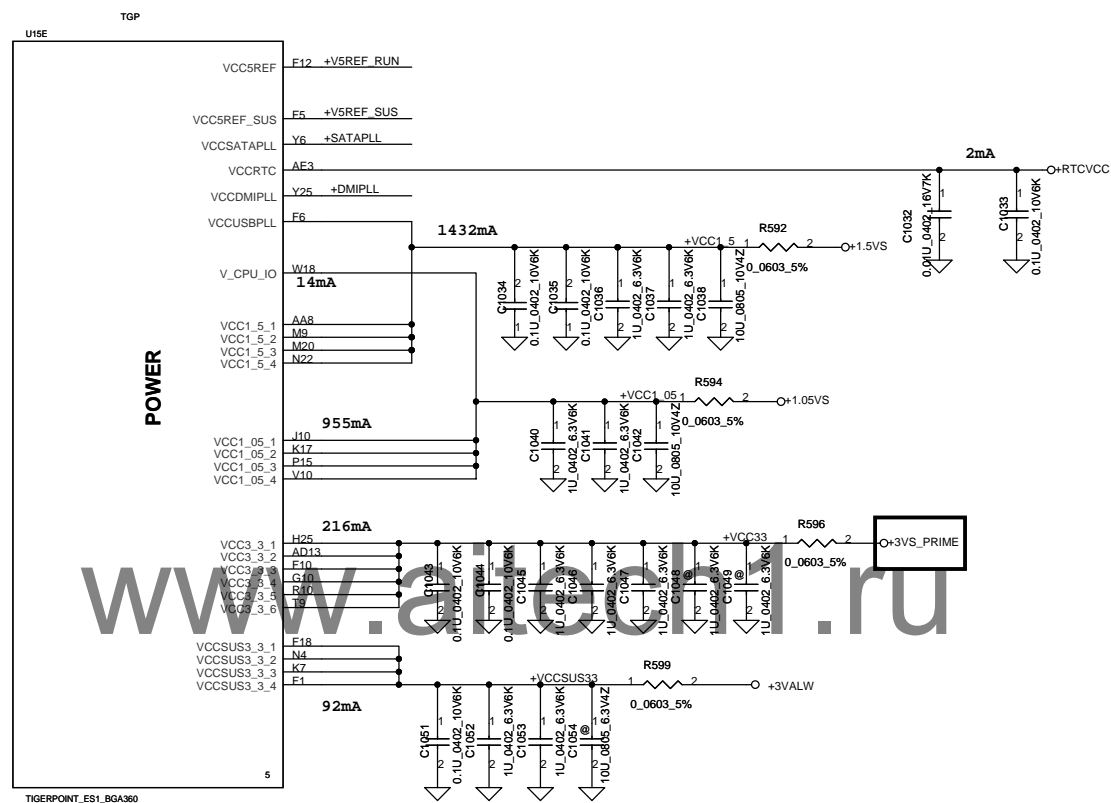
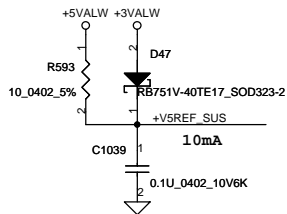
01/11 Reserve EC\_CLK for KBC

8/24 Add R254 pull down for EC request



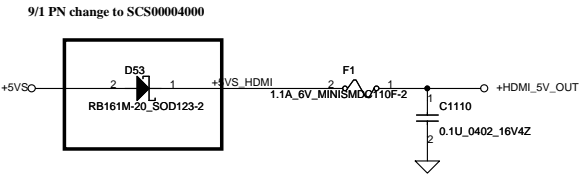
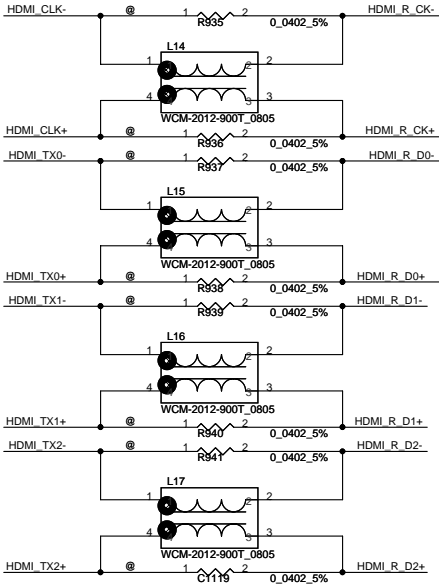
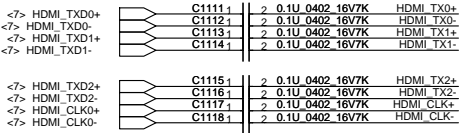
2010.03.22 Un-stuff RSMRST# circuit and use 0 ohm bypass

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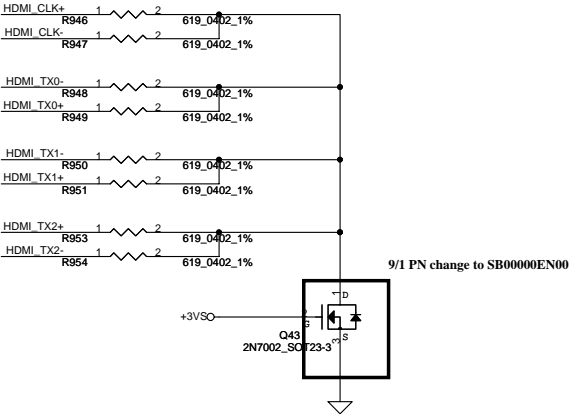
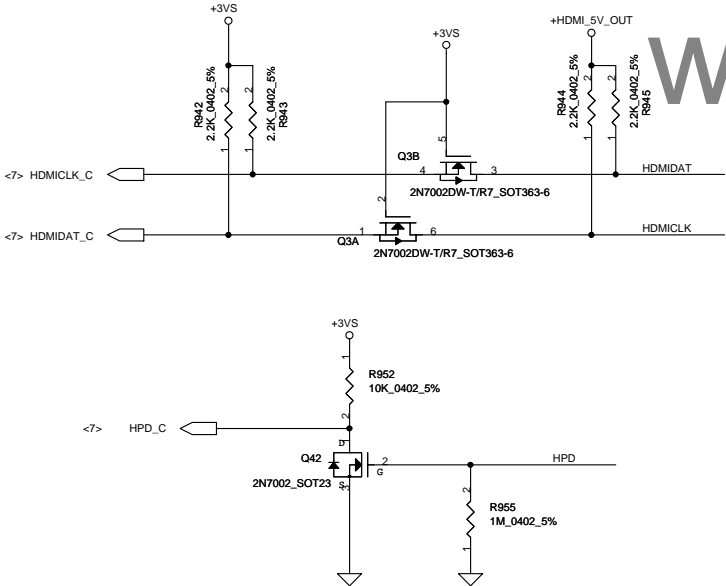
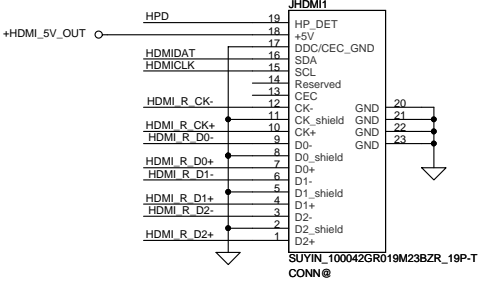


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HDMI CONNECTOR



< HDMI Connector >

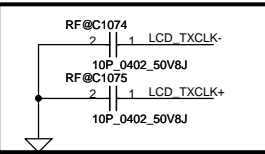
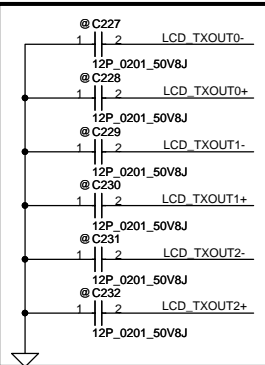


9/1 PN change to SB000000EN00

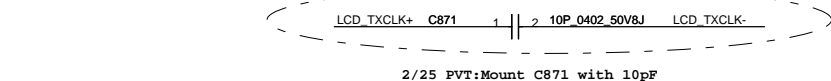
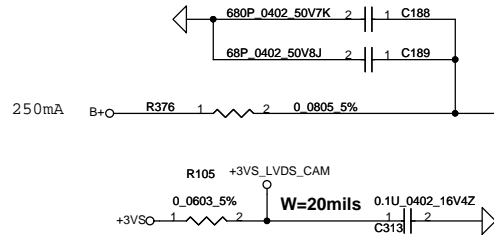
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Issued Date		2010/06/27		Deciphered Date		2011/6/27		Title		SCHEAMTIC MB A6856			
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# LCD POWER CIRCUIT

# MP Add C227~C232 for RF request

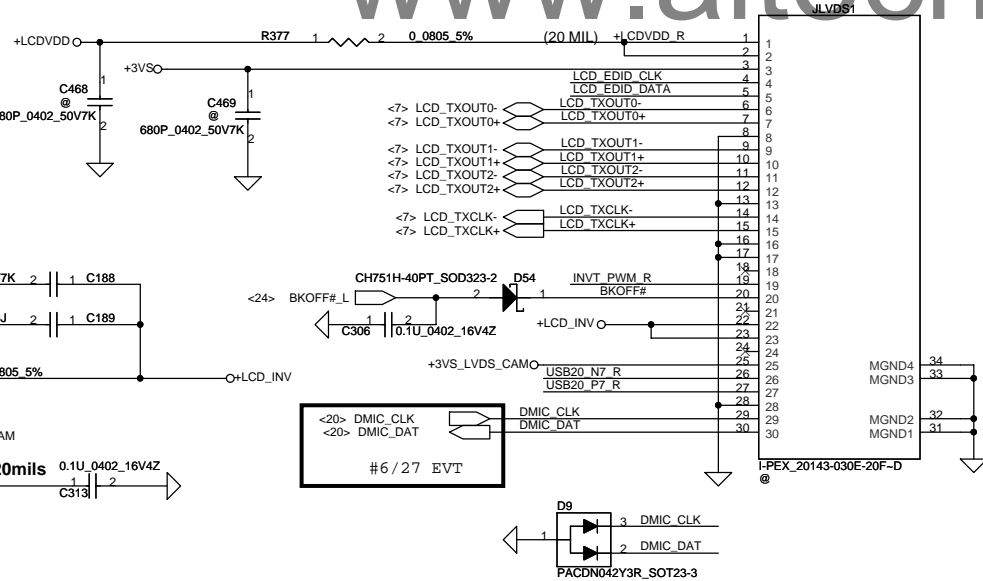
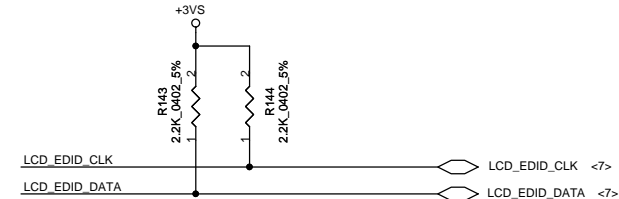
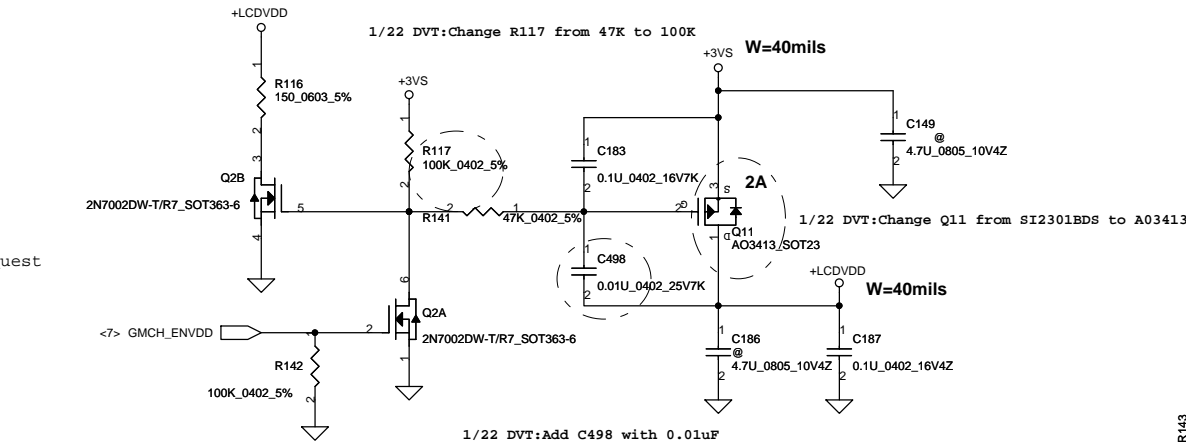


# PVT Add C1074, C1075 10p and stuff for RF

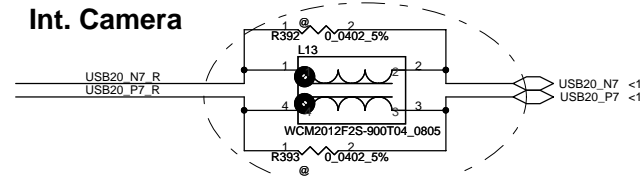


LED/PANEL BD. Conn.

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Int. Camera



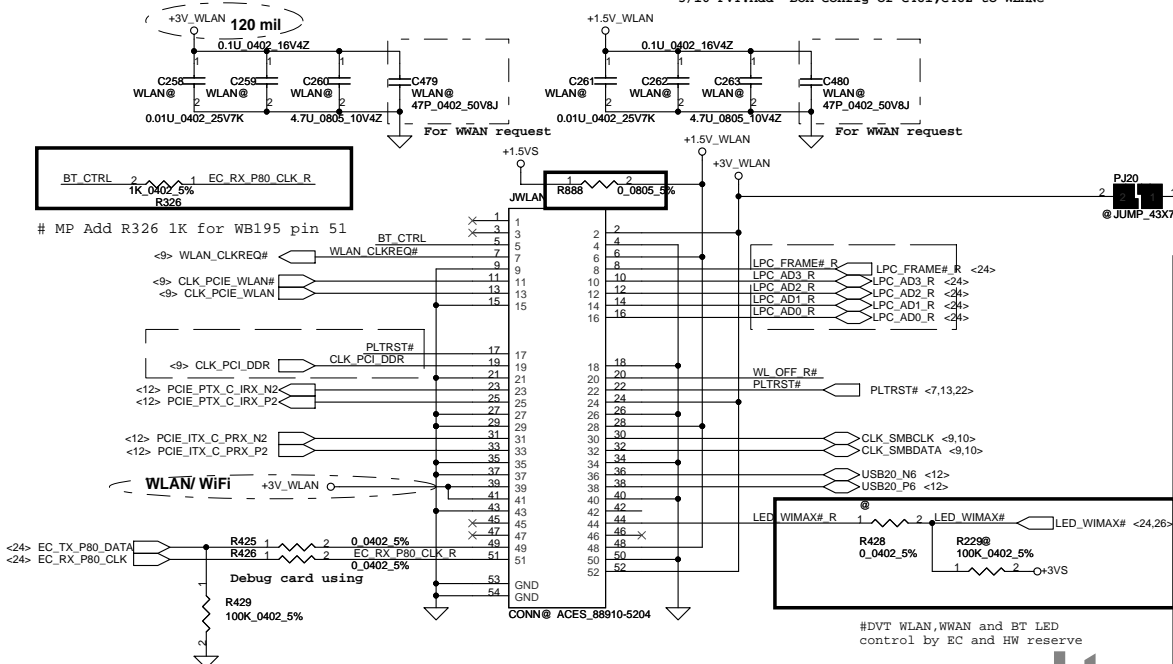
For EMI request

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## Mini-Express Card for WLAN/WiMax

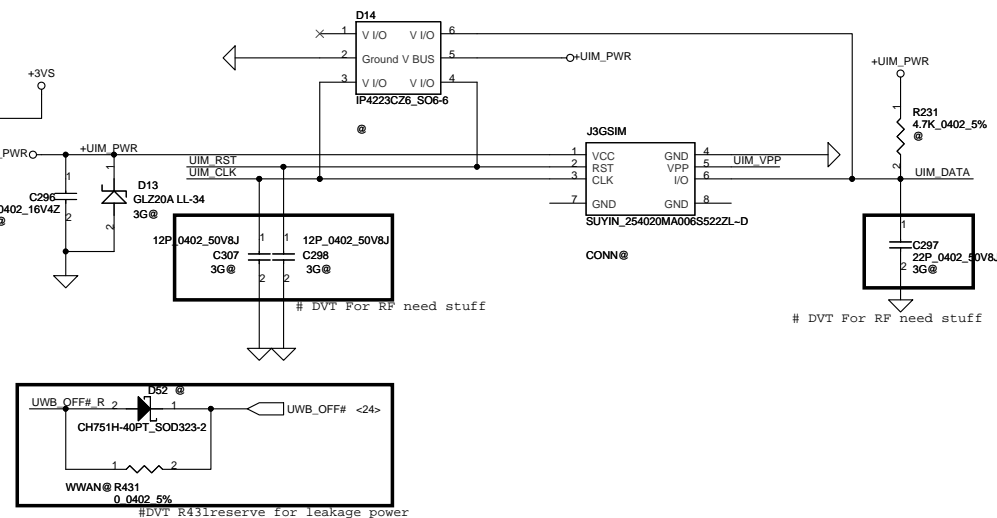
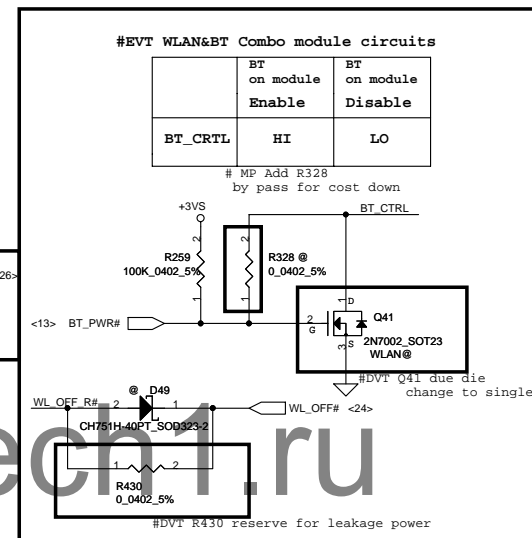
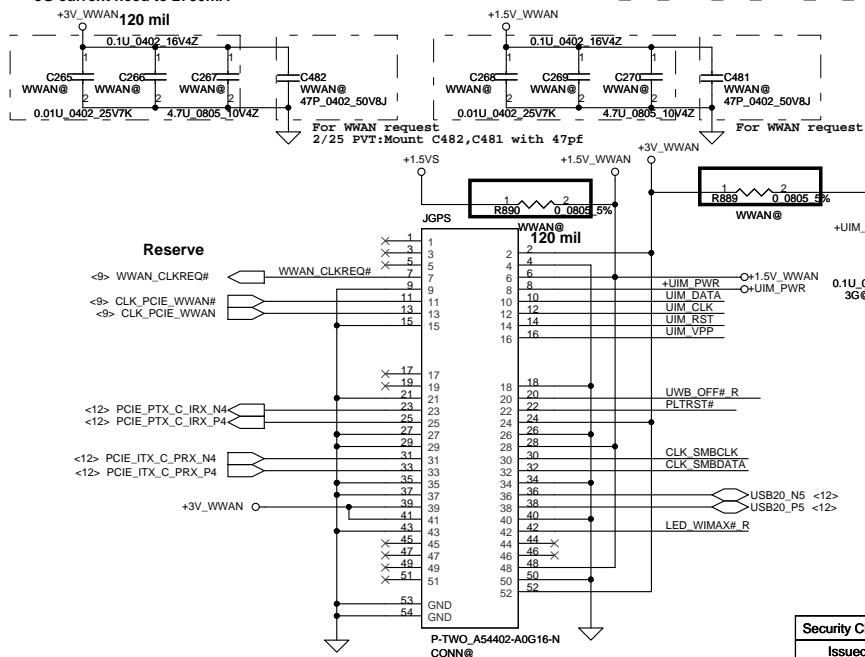
```
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@
```



## Mini-Express Card for 3G/GPS

3G current need to 2750mA

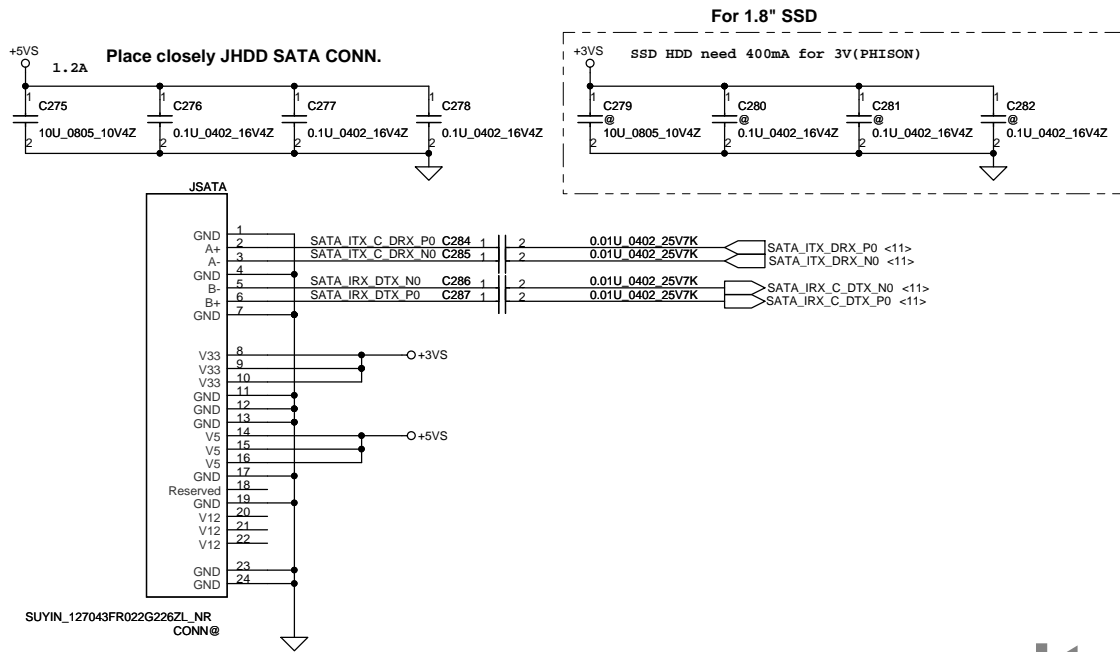
3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@



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# SATA Conn.

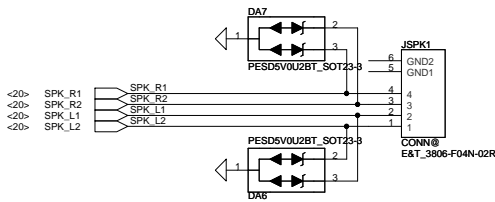


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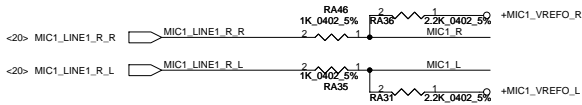
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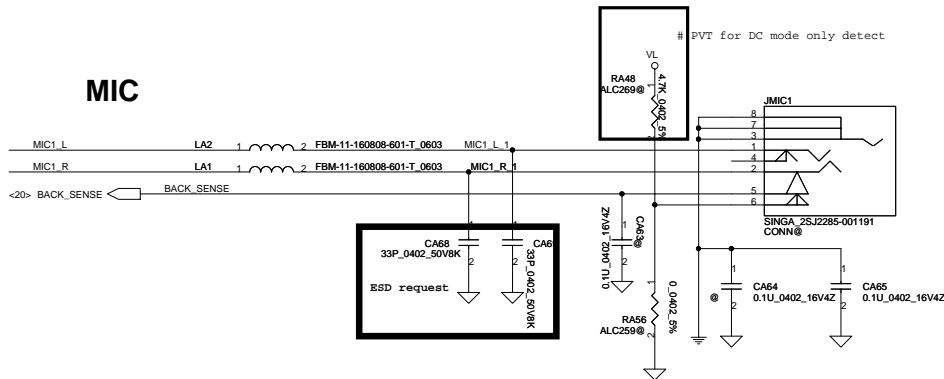
SPEAKER



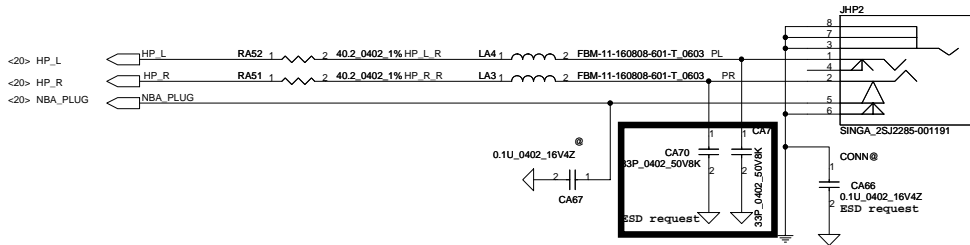
Ext.MIC/LINE IN JACK



MIC



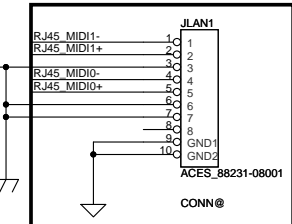
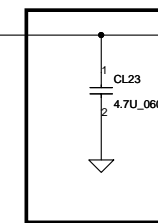
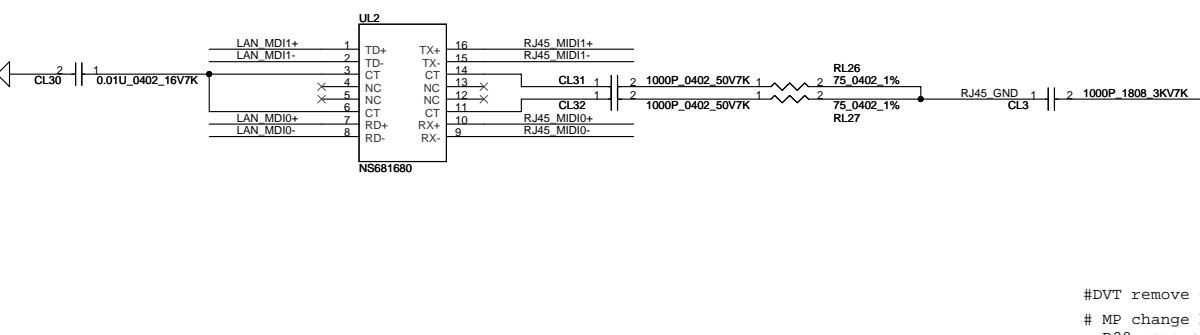
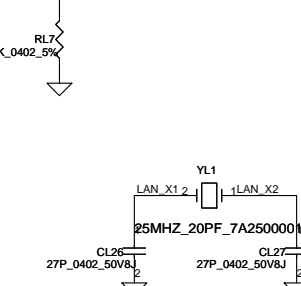
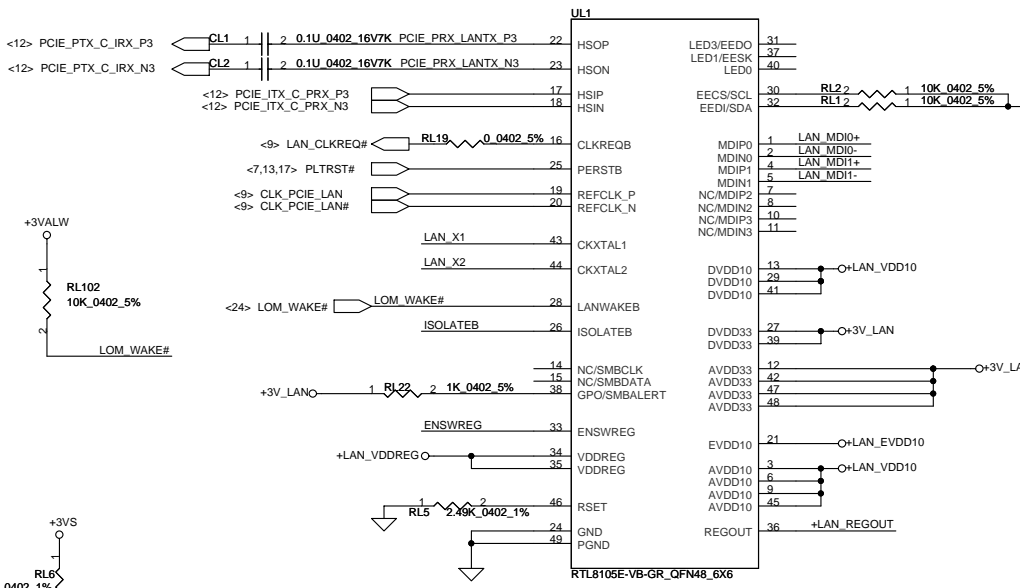
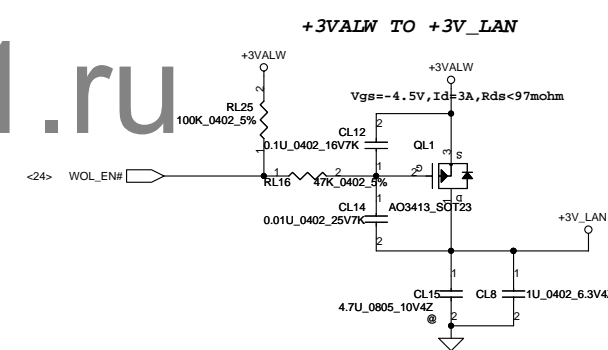
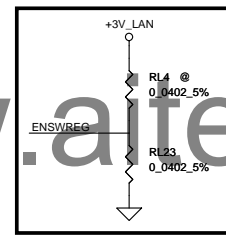
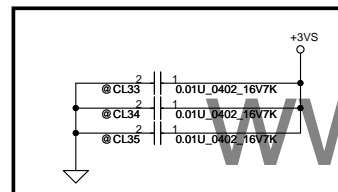
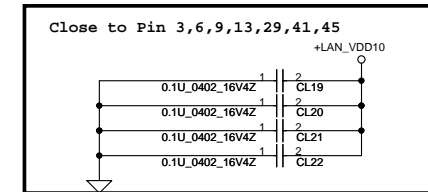
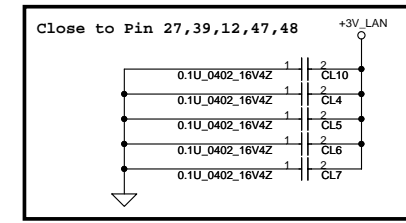
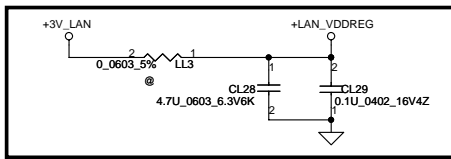
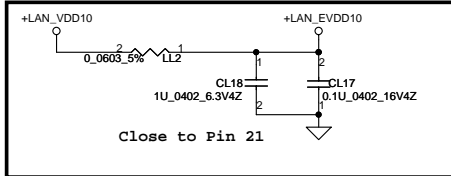
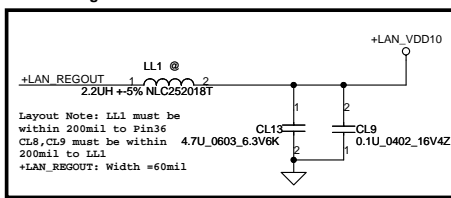
Head phone



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# 3/10 Change CL13 0805-->0603

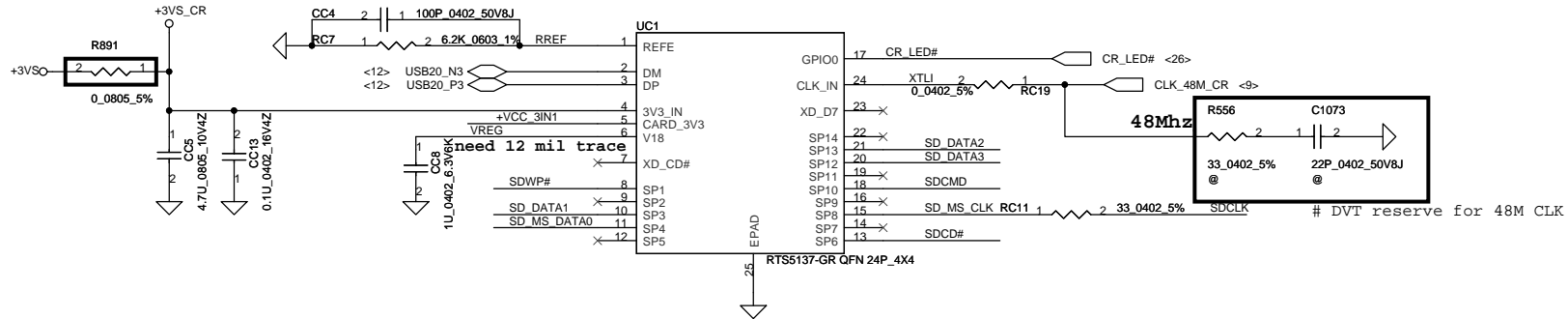


#DVT remove CL16 and CL23, Add ESD diode  
# MP change back to original design for EMI  
D28 remove and add CL23 4.7U

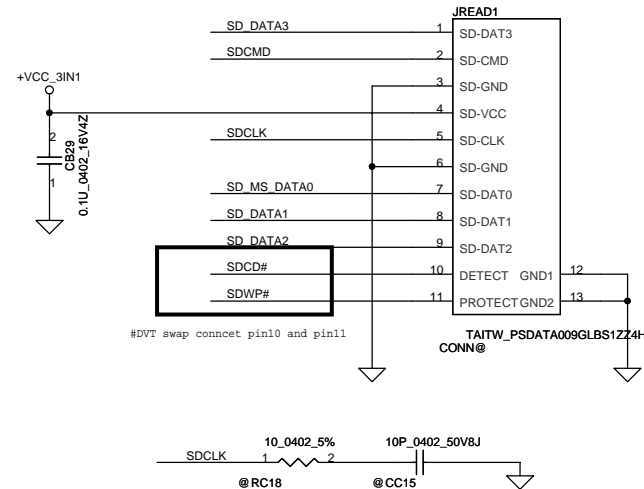
#DVT LAN connect pin defind change  
# PVT Add pin 7 connect to LANGND

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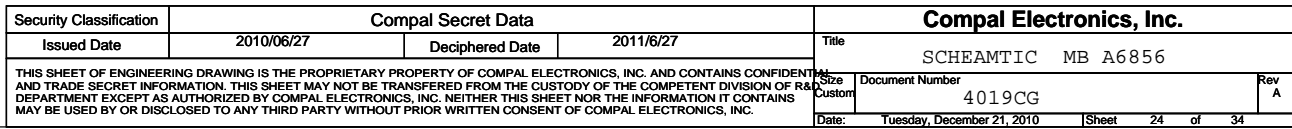
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_C#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



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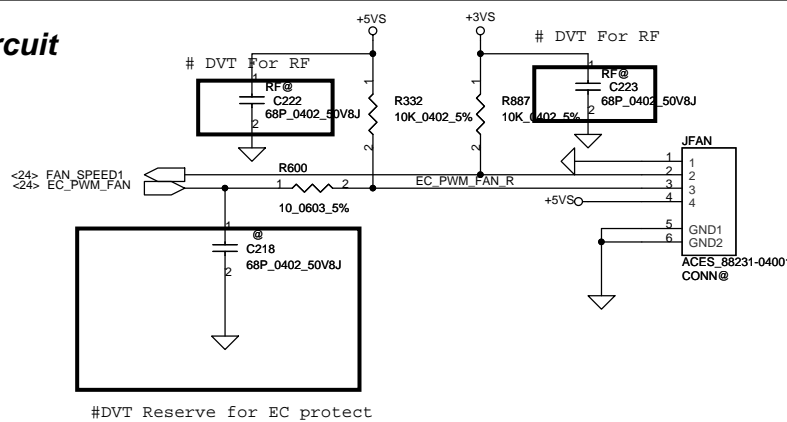


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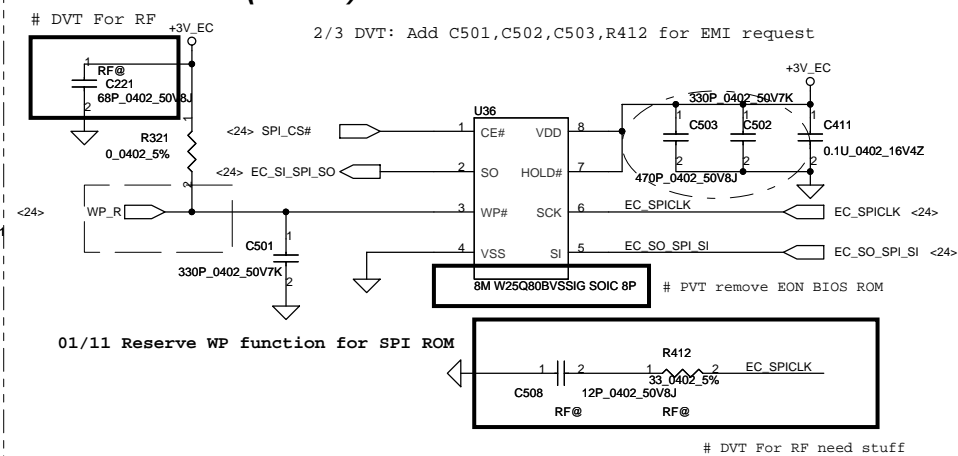




## FAN Control Circuit



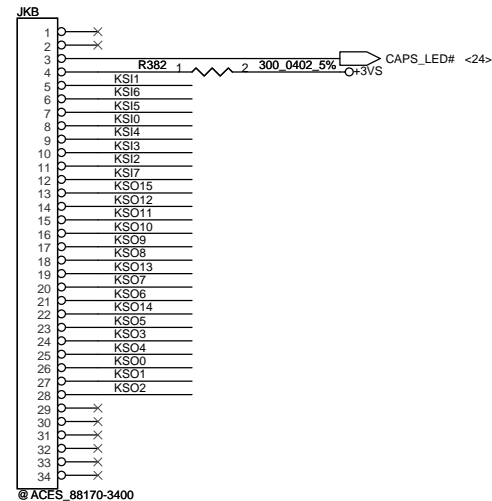
## SPI Flash (8Mb\*1)



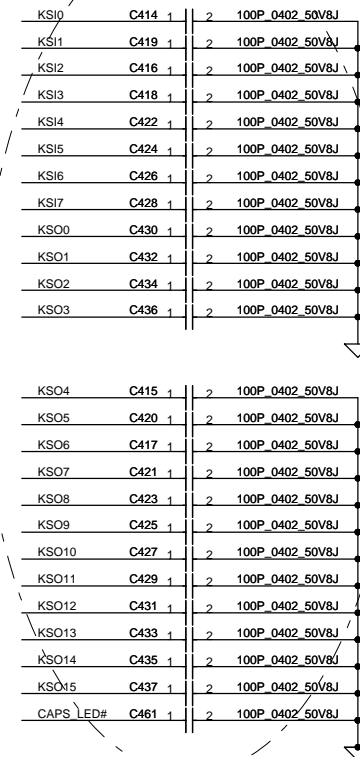
## LPC Debug Port

## KEYBOARD CONN.

KSIO[0..7] <24>  
KSO[0..15] <24>



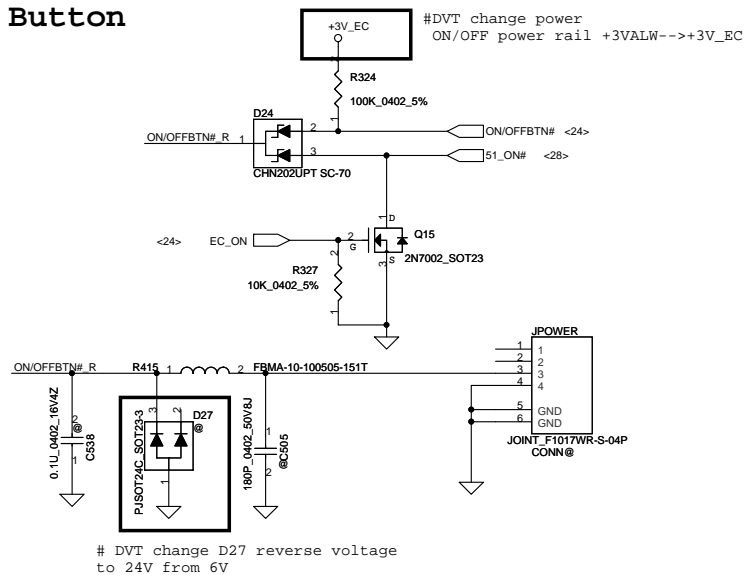
12/18 Follow KB Matrix the same to KSKAA



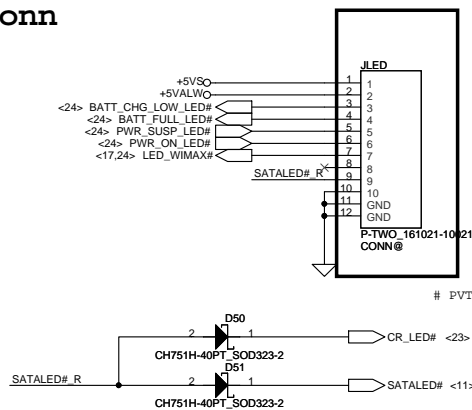
3/4 PVT:Mount C414~C437,C461 for EMI request

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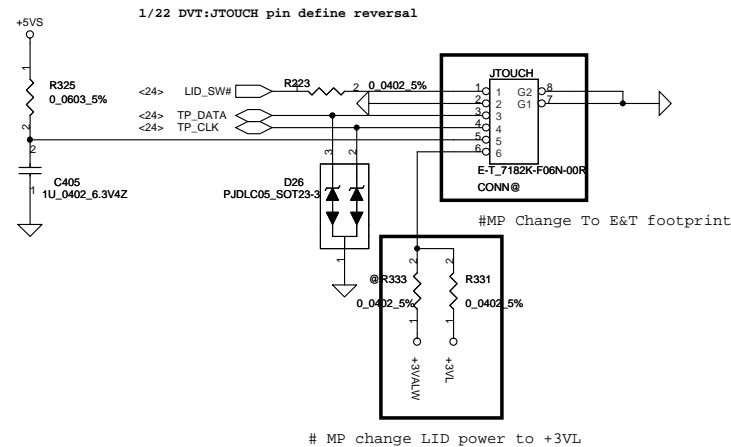
## Power Button



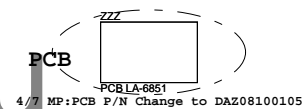
## LED Conn



## Touch/B Connector



**ISPD**



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**VALW**

Vgs=-0V, Id=9A, Rds=18.5mohm

4/2 MP:For EMI ESD solution

Si7326DN-T1-E3\_PAK1212-8  
Q18

C439 1U\_0402\_6.3V4Z

C440 4.7U\_0805\_10V4Z

R342 470\_0805\_5%

+VSB

R344 47K\_0402\_5%

SUSP.

Q6A 2N7002DW-T/R7\_SOT363-6

Q6B 2N7002DW-T/R7\_SOT363-6

R348 330K\_0402\_5%

C446

C447 0.022U\_0402\_16V7K

ESD solution

2/25 PVT:Change C447 with 0.022uF

[illegible]

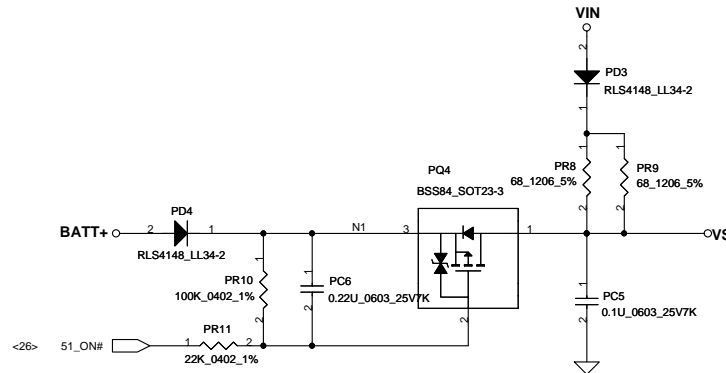
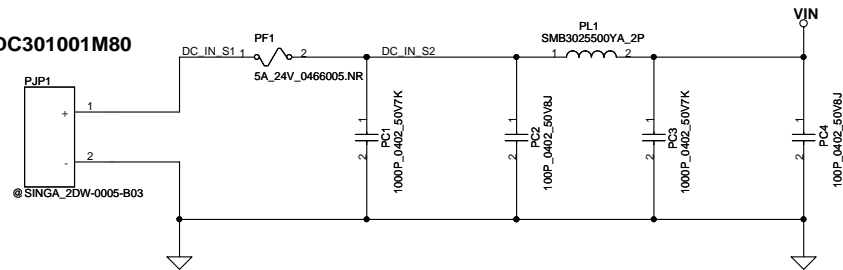
8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

8/14 R237 for HW design

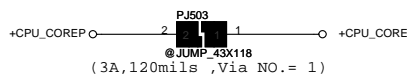
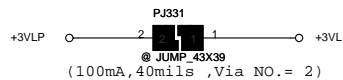
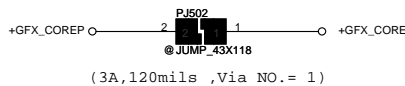
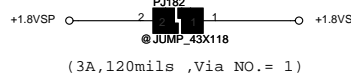
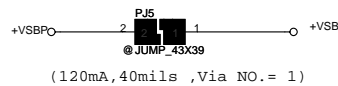
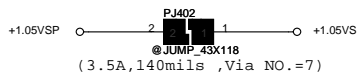
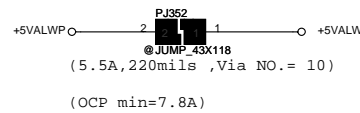
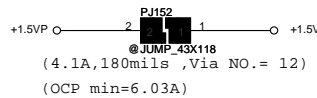
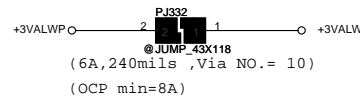
7/9 Add Q29, Q30, R228 for Intel power sequence

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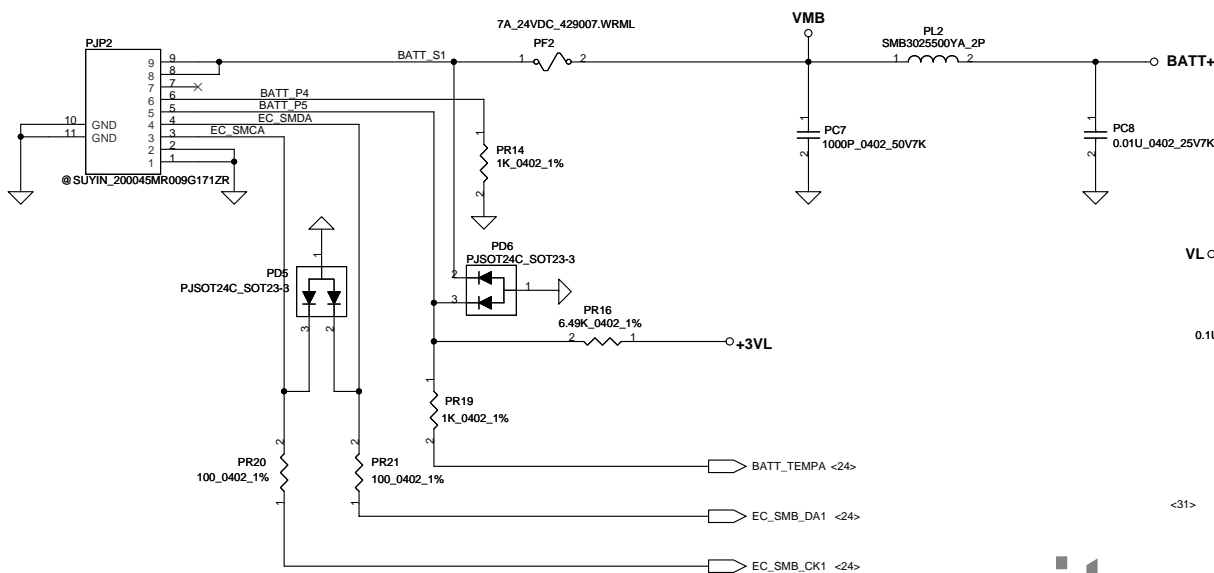
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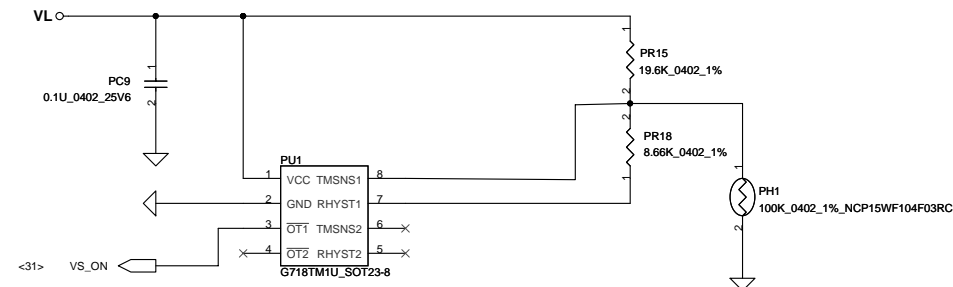
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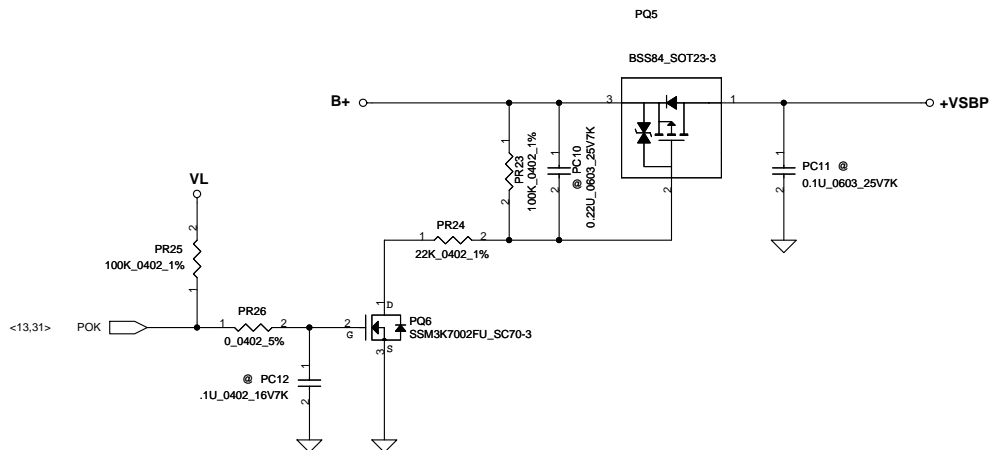
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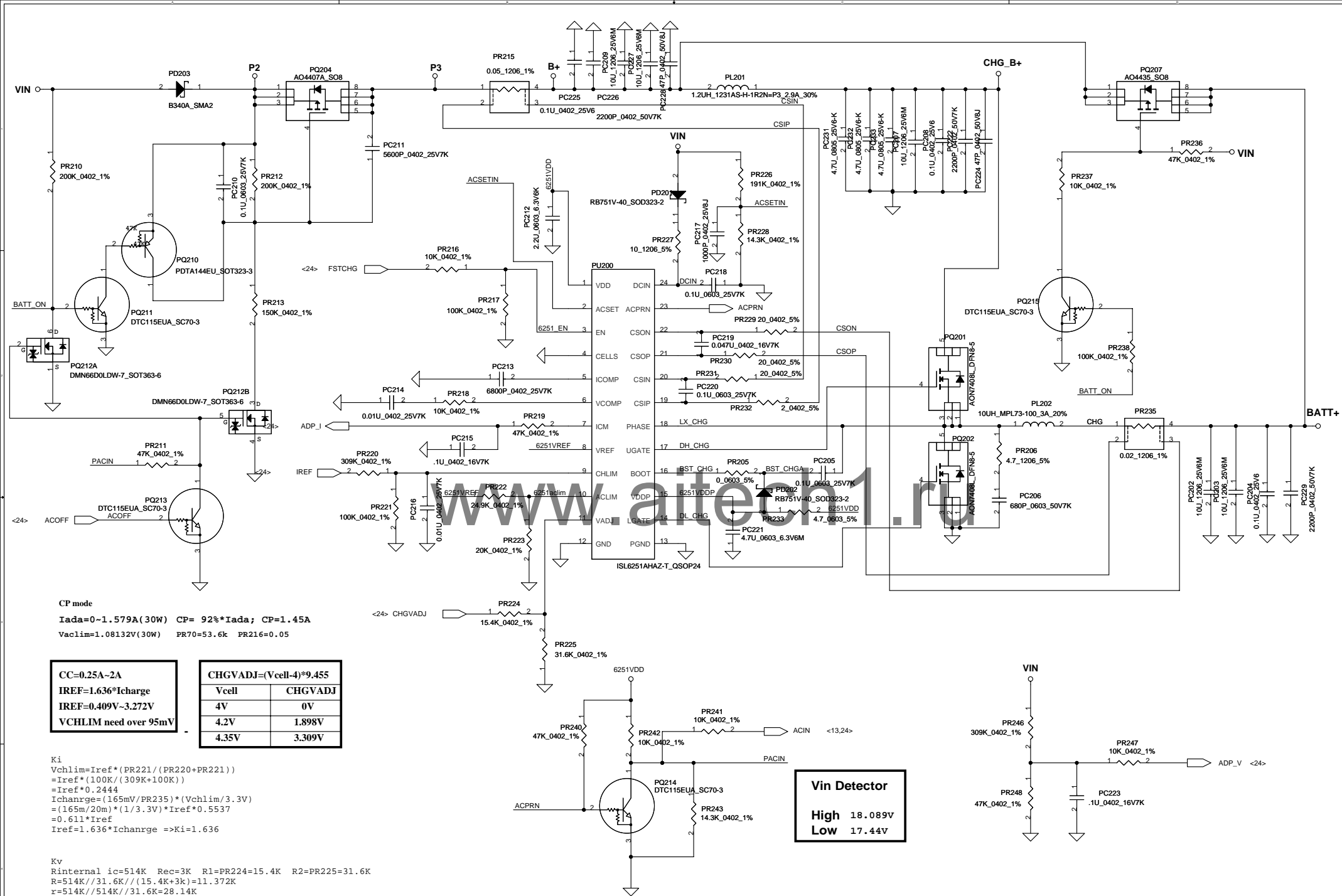
PH1 under CPU botten side :  
CPU thermal protection at 95 degree C  
Recovery at 56 degree C

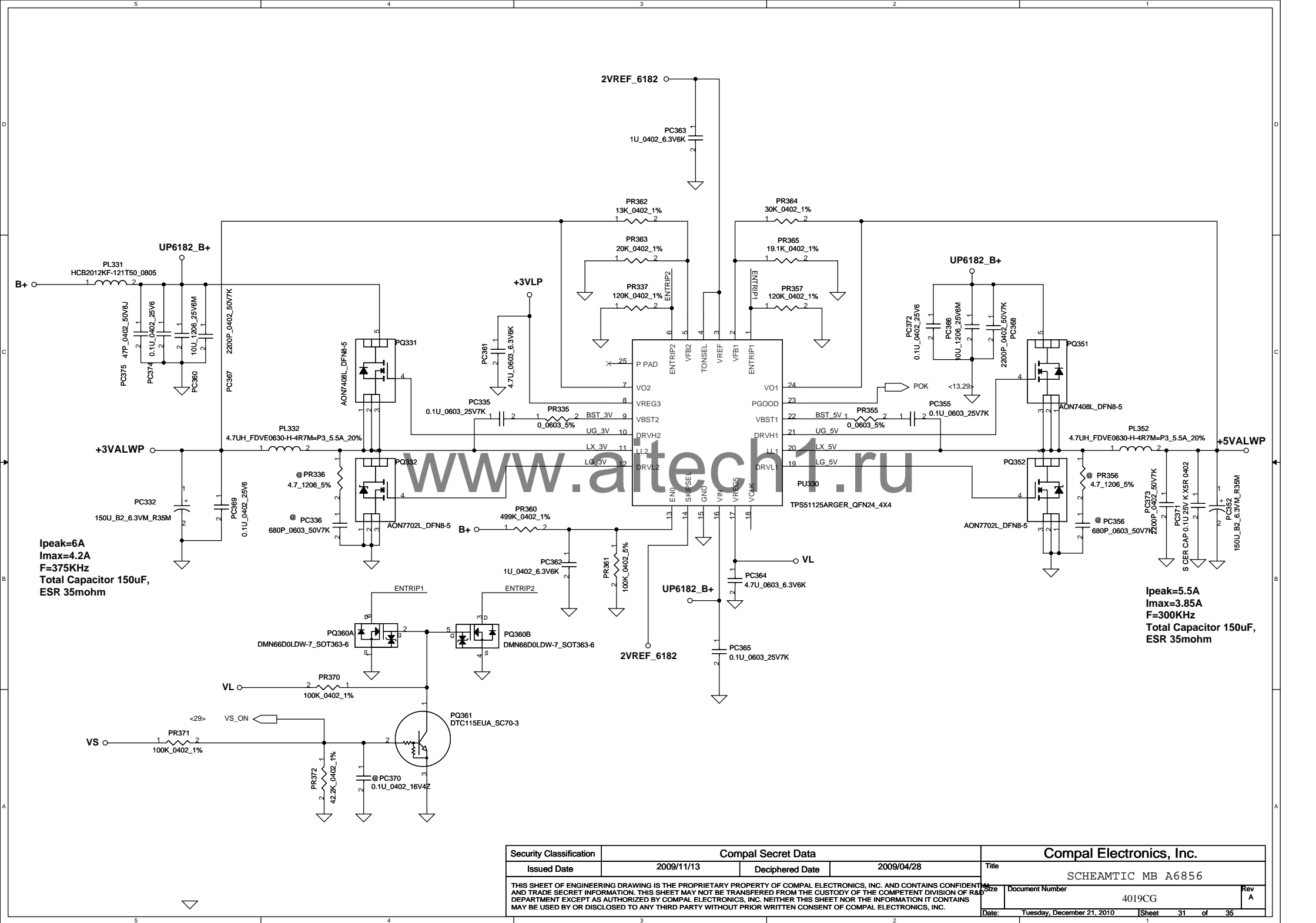


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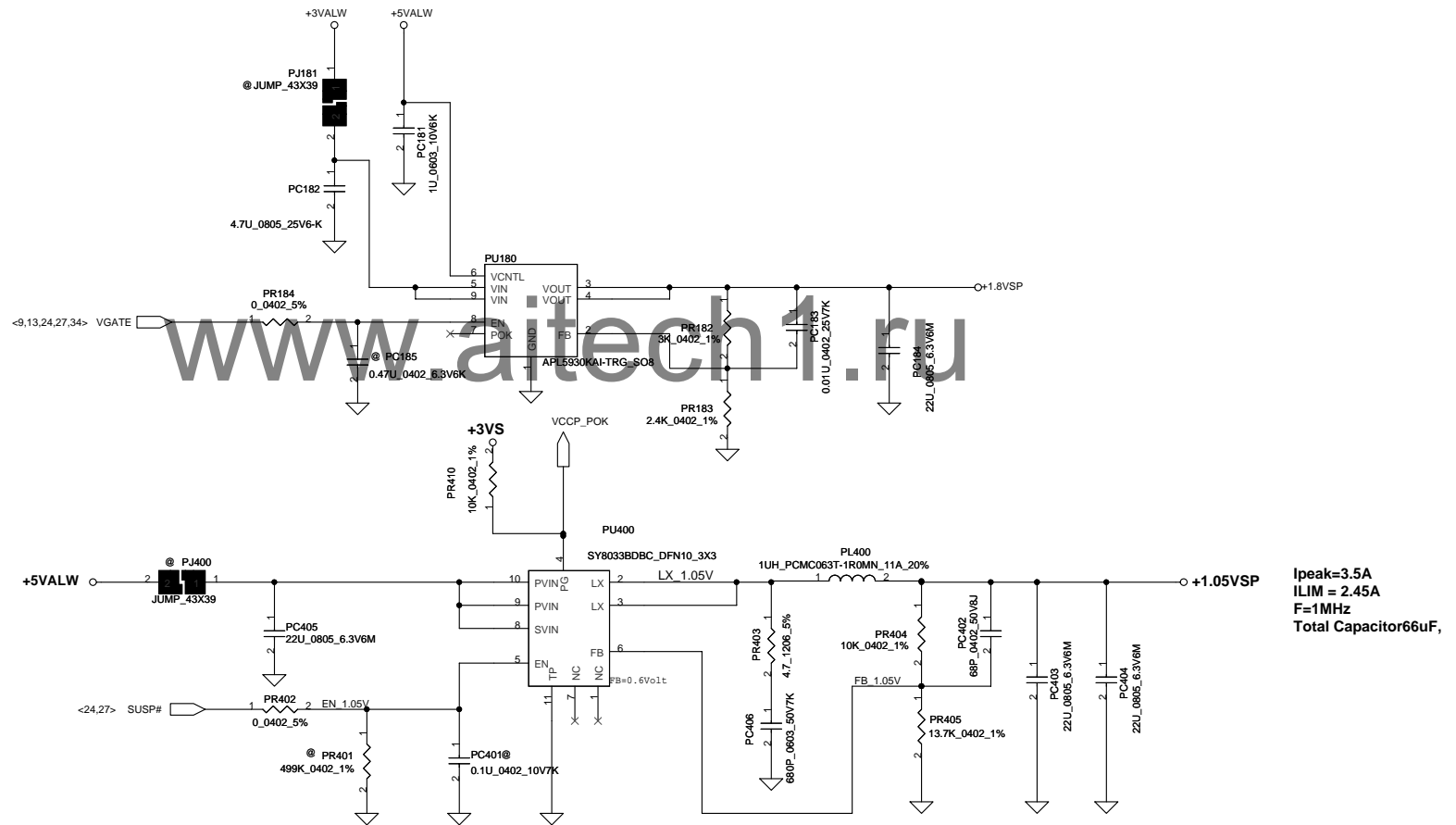




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Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,  
SY8035 is for 5A loading , let LX shape can bigger!!

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